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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,589	02/13/2001	David Andrew Mc Connell	ATML04US	9482

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EXAMINER	
SHAAWAT, MUSSA	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/782,589	MC CONNELL ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- *Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.*
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13 February 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application number 09/782,589. Claims 1-6 are presented for examination. Claims 1-3 teach a method for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC). Claims 4-6 teach a system for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. All the claims recite the term "simulator-port layout" but there is no description in the claims or the specification as to what a "simulator-port layout" consist of. In explaining the steps in figure 3 the specification mentions the "simulator-port layout", block 47, but does not define what this block really accomplishes or consist of. This is a critical item since all the claims mention "simulator-port layout" but there is a lack of definition and an artisan of ordinary skill would be unable to understand or implement this feature. The steps required to produce the "simulator-port layout" critical to the invention are also not described.

4. Further claims 1 and 4 specify, "simulating in hardware a FPSLIC device". These are not specific and would be confused to the artisan trying to implement the invention as to what is the

object of the simulation. The examiner suspects that it is the function that has been personalized or configured into the FPSLIC device rather than the device proper that is to be simulated.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 1 and 4 verify contents of the "simulator-port layout" using the register contents. Claims 2 and 5 verifies the contents from the "simulator-port layout" using peripheral contents. Claims 3 and 6 verify the contents from the "simulator-port layout" using UART layout. There is insufficient antecedent basis in the specification that describes what constitutes the "contents" of any of these devices or how they correlate to the verification of the "simulator-port layout". An artisan most familiar with the simulation/emulation arts would not know how to implement these functions based on the descriptions in the specification or in the claims. The artisan would not know what to include and what to exclude in verifying the "simulator-port layout" with respect to the contents of any of these devices.

8. In addition claims 1-6 are rejected as being indefinite because they include devices not defined in the specification or in the claim language. The term "register" in claims 1 and 4, the term "peripheral" in claims 2 and 5 and the term "UART" in claims 3 and 6 are not identified in the specification such that an artisan most familiar with the simulation/emulation arts would know what is included and what is excluded by these limitations in the language.

9. The examiner will interpret the claims as comprising a co-verification method that utilizes a software model for logic simulation of a design and utilizes reconfigurable hardware to emulate a hardware model of the design.

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claim(s) 1-18 of Patent No. (6,272,451) contain(s) every element of claim(s) 1-6 of the instant application and as such anticipate(s) claim(s) 1-6 of the instant application.

A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225

USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

12. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of the '451 US Patent. Although the conflicting claims are not identical, they are not patentably distinct from each other. The term simulator-post layout in claim1 of the '451 US Patent is omitted from claim 1 of the instant application and is replaced by the term simulator-port layout. It would have been obvious, by one of ordinary skill in the art, at the time of the invention, to modify the terms of claim 1 of the instant application as indicated above since the omission or addition of the terms in claim 1 of the instant application would have not changed the process of the invention. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson,* 136 USPQ 184 (CCPA 1963).

13. Claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of the '451 US Patent. Although the conflicting claims are not identical, they are not patentably distinct from each other. The term simulator-post layout in claim 2 of the '451 US Patent is omitted from claim 2 of the instant

application and is replaced by the term simulator-port layout. It would have been obvious, by one of ordinary skill in the art, at the time of the invention, to modify the terms of claim 2 of the instant application as indicated above since the omission or addition of the terms in claim 2 of the instant application would have not changed the process of the invention. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson,* 136 USPQ 184 (CCPA 1963).

14. Claim 3 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 and claim2 of the '451 US Patent. Although the conflicting claims are not identical, they are not patentably distinct from each other. The term simulator-post layout in claim 1 and 3 of the '451 US Patent is omitted from claim 3 of the instant application and is replaced by the term simulator-port layout. It would have been obvious, by one of ordinary skill in the art, at the time of the invention, to modify the terms of claim 3 of the instant application as indicated above since the omission or addition of the terms in claim 3 of the instant application would have not changed the process of the invention. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson,* 136 USPQ 184 (CCPA 1963).

15. Claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2 and 3 of the '451 US Patent. Although the conflicting claims are not identical, they are not patentably distinct from each other. The term simulator-post layout in claim 1, 2 and 3 of the '451 US Patent is omitted from claim 4 of the

instant application and is replaced by the term simulator-port layout. It would have been obvious, by one of ordinary skill in the art, at the time of the invention, to modify the terms of claim 4 of the instant application as indicated above since the omission or addition of the terms in claim 4 of the instant application would have not changed the process of the invention. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson,* 136 USPQ 184 (CCPA 1963).

16. Claim 5 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2 and 3 of the '451 US Patent. Although the conflicting claims are not identical, they are not patentably distinct from each other. The term simulator-post layout in claim 2 and 3 of the '451 US Patent is omitted from claim 5 of the instant application and is replaced by the term simulator-port layout. It would have been obvious, by one of ordinary skill in the art, at the time of the invention, to modify the terms of claim 5 of the instant application as indicated above since the omission or addition of the terms in claim 5 of the instant application would have not changed the process of the invention. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson,* 136 USPQ 184 (CCPA 1963).

17. Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of the '451 US Patent. Although the conflicting claims are not identical, they are not patentably distinct from each other. The term simulator-post layout in claim 3 of the '451 US Patent is omitted from claim 6 of the instant application and is

replaced by the term simulator-port layout. It would have been obvious, by one of ordinary skill in the art, at the time of the invention, to modify the terms of claim 6 of the instant application as indicated above since the omission or addition of the terms in claim 6 of the instant application would have not changed the process of the invention. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson,* 136 USPQ 184 (CCPA 1963).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Sample et al. US Patent No. (5,841,967) referred to hereinafter as Sample.

19. As to claim1, Sample teaches a method for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC) and a software simulation of the field-programmable-system-level integrated circuit, comprising the steps of: simulating in hardware a FPSLIC device, see Sample (col.5 lines 1-10); generating, from the simulation in hardware, a simulator-port layout of the FPSLIC device, see Sample (figure 13 reference # 140, col. 1 lines 43-47); simulating, with an instruction-set simulator, in software the FPSLIC device, see Sample

(col.13 lines 55-67); outputting register contents from the instruction-set software, from the simulation in software; and verifying contents from the simulator-port layout with the register contents, see Sample (Abstract).

20. As to claim 2, Sample teaches a method of co-verification of a design, similar to the instant application that simulates a logic model using a computer and emulates a hardware model that has been loaded into reconfigurable FPLA devices. Regarding the use of contents in the verification process applicant is reminded that in a co-verification process, the result of the simulation and emulation need to be communicated back and forth between the software and hardware models. This is an inherent design requirement since there are values, which must be shared between the models to keep the models in synchronization (see Sample, column 6 lines 42-50). Sample uses a bus for this purpose (see figure 2 item 18) but suggest that a network can be used (column 3 lines 28-40). Communication of data between the models is a necessary design requirement and the method used to transfer the required quantities would be a design dependent decision to which the examiner gives no weight concerning the inventive subject matter.

21. As to claim 3, Sample teaches a method of co-verification of a design, similar to the instant application that simulates a logic model using a computer and emulates a hardware model that has been loaded into reconfigurable FPLA devices. Regarding the use of UART contents in the verification process, applicant is reminded that in a co-verification process, the result of the simulation and emulation need to be communicated back and forth between the software and hardware models. This is an inherent design requirement since there are values, which must be shared between the models to keep the models in synchronization (see Sample, column 6 lines

42-50). Sample uses a bus for this purpose (see figure 2 item 18) but suggest that a network can be used (column 3 lines 28-40). Communication of data between the models is a necessary design requirement and the method used to transfer the required quantities would be a design dependent decision to which the examiner gives no weight concerning the inventive subject matter.

22. As to claim 4, claim 4 include similar limitations of claim 1, therefore it is rejected based on the same rationale, supra.

23. As to claim 5, claim 5 include similar limitations of claim 2, therefore it is rejected based on the same rationale, supra.

24. As to claim 6, claim 6 include similar limitations of claim 3, therefore it is rejected based on the same rationale, supra.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Huang US Patent No. (5,563,829) Multi-port memory emulation using tag registers
- Mohsen US Patent No. (5,544,069) Structure having different levels of programmable integrated circuits interconnected through bus lines for interconnecting electronic components.
- Matsuoka et al. US Patent No. (5,960,182) Hardware software co-simulation system, hardware-software co-simulation method, and computer readable memory containing a hardware-software co-simulation program.

- Klein US Patent No. (5,771,370) Method and apparatus for optimization hardware and software co-simulation.
- Graves et al. US Patent No. (5,946,472) Apparatus and method for performing behavioral modeling in hardware emulation and simulation environments.
- Aihara US Patent No. (5,987,243) Hardware and software co-simulator and its method.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (703) 605-1372. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (703) 308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Examiner
August 31, 2004

JEAN R HOMERE
PRIMARY EXAMINER